REMARKS

Claims 1, 4-11, and 13-20 are all the claims pending in the application. Claims 2, 3, and 12 are canceled herein without prejudice or disclaimer. Claims 2-20 stand rejected upon informalities. Claims 1, 2, 5, 7-11, 14 and 16-18 stand rejected on prior art grounds. Claims 1, 5, 10, 14, 16-18, and 20 are amended herein as well as the drawings. No new matter is being added. In addition, the drawings and specification are objected to. The Applicant respectfully traverses these objections/rejections based on the following discussion.

I. The Objections to the Specification

The specification is objected to because, according to the Office Action, in pages 9-13, it is not clear what the "notation" (I^1/4s) represents. The Applicant has reviewed the entire specification and cannot find any such notation. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this objection.

Furthermore, the Office Action requires further explanation as to how the analog cycle can be overlapped with the digital cycle. The Office Action suggests that there is no cycling function of the circuit between the analog configuration and the digital configuration. The Applicant respectfully traverses this objection based on the following discussion.

As clearly stated on page 16, lines 8-14 of the specification as filed, "Figure 7 shows two comparison cycles with each cycle approximately 31 μs in duration. In the first comparison cycle between times 0 μs and 31 μs, the inventive comparator is in the analog configuration between time 0 μs to 5 μs and time 30 μs to 31 μs for a total of 6 μs, and in the digital configuration between time 5 μs and 30 μs for a total of 25 μs. This clearly shows that the

comparator is in the power saving digital mode for more than 80% of the comparison cycle time." (emphasis added). Therefore, there is no overlapping as the Office Action suggests, rather, the comparator is in the analog cycle between time 0 μs to 5 μs, in the digital cycle between time 5 μs and 30 μs, and then in the analog cycle between time 30 μs to 31 μs. Thus, there clearly is a cycling function between the analog and digital cycles; i.e., the comparator cycles from analog to digital and back to analog.

Furthermore, as indicated on page 8, lines 19-22 through page 9, lines 1-17 of the specification as originally filed:

> The inventive comparator can be considered analog for part of the cycle and digital for the remainder of the cycle, making it ideal for use in low power applications. The distinction between the analog and digital configurations is determined, in large part, by the presence or absence of static DC current paths as well as the region of operation of the transistors. In the analog configuration, there are static DC current paths present and certain transistors operate in the region known as saturation. In the digital configuration, static DC current paths are absent and the transistors are either operating in the linear (triode) region or cutoff region. When the input signal COMPIN rises from GND toward V_{CC}, the tail current source transistor T1 switches on.
>
> In Figure 1, when the comparator input signal COMPIN is of sufficiently low voltage, the comparator is in the analog configuration since there is static DC current flowing through tail current source transistor T1, continuing through transistors (T2 and T4) and/or transistors (T3 and T5) to GND. In this situation, transistors T2, T3, T4, and T5 are generally in saturation. Figures 3 and 4, as will be described later, depict the inventive comparator in the analog configuration.
>
> When the comparator input signal COMPIN is of sufficiently high voltage, the comparator is in the digital configuration since there is no static DC current flowing and the transistors are operating either in the linear (triode) region or in the cutoff region. Specifically, transistors T1, T2, and T5 are in cutoff while transistors T3 and T4 are in the linear (triode) region. Figures 5 and 6, as will be described later, depict the inventive comparator in the digital configuration.

Moreover, as indicated on page 12, lines 7-18 of the specification as originally filed:

> Figure 3 shows an analog illustration of Figure 2, whereby the transmission gates have been removed and replaced by either an open circuit or short circuit. Inverters INV1 and INV2 have been omitted as well because their outputs are only used as inputs to the now deleted transmission gates. Figure 4 shows an alternate representation of Figure 3, whereby all dangling nets or stubs have been removed to aid in the understanding of the circuit more completely. Figure 4 represents the analog configuration of the inventive comparator of Figure 1, wherein there is static DC current flow, and transistors T2, T3, T4, and T5 operate predominantly in the saturation region. In this configuration, the gate of PMOS tail current transistor T1 is shorted to GND potential which turns it on and allows static DC current to flow from V_{CC} through T1 into the PMOS differential pair transistors T2/T3 and onto GND through current mirror load transistors T4/T5. This analog transformation is essentially a differential pair in an open loop configuration with a current mirror load.

Additionally, as indicated on page 14, lines 1-13 of the specification as originally filed:

> This is further depicted in Figure 5, which shows the digital configuration of Figure 2, and where the transmission gates have been removed and replaced with either an open or short circuit. Moreover, the input signal COMPIN is at an input voltage greater than the external reference voltage V_{REF}. Inverters INV1 and INV2 have been removed for clarity as well. Furthermore, Figure 6 illustrates an alternate representation of Figure 5, whereby all dangling nets or stubs have been removed to aid in the understanding of the circuit more completely. Additionally, in Figure 5, a short circuit exists across transistor T5, which is why it is not present in Figure 6. Also in Figure 5, the V_{REF} pin is unconnected and, therefore, it is not represented in Figure 6. Figure 6 further represents the digital configuration of the inventive comparator of Figure 1 because there are no static DC current paths, and transistors are operating in either the linear (triode) or cutoff regions. As a result, in this configuration, minimal power is being dissipated which makes the present invention ideal for low power applications. Furthermore, Figure 6 provides the characteristics of an asymmetric inverting Schmitt trigger.

The above language clearly articulates the analog and digital aspects of the comparator.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this objection.

II. The Objections to the Drawings

The drawings are objected to under 37 CFR §1.83(a). According to the Office Action, the "analog circuit", "digital circuit", "a first portion", "a second portion", "an input signal source", "an output signal source", and "an external input signal source" must be shown in the drawings. The Applicant respectfully traverses this objection based on the following discussion.

The above features are all clearly shown in the drawings. The "analog circuit", which is the "first portion" is shown in Figures 3 and 4. That is, the circuits shown in Figures 3 and 4 are each the "analog circuit" otherwise referred to as the "first portion". The "digital circuit", which is the "second portion" is shown in Figures 5 and 6. That is, the circuits shown in Figures 5 and 6 are each the "digital circuit" otherwise referred to as the "second portion". The "input signal source" is represented as "COMPIN" in Figures 1-6. The "output signal source" is represented as "COMPOUT" in Figures 1-6. The "external input signal source" is represented as "V_{REF}" in Figures 1-5. Moreover, those skilled in the art of electrical circuit design readily accept such terminology and the corresponding designations. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw these objections.

III. The 35 U.S.C. §112, Second Paragraph Rejections

Claims 2-20 stand rejected under 35 U.S.C. §112, second paragraph. The Applicant respectfully traverses this objection based on the following discussion. As mentioned previously, and as clearly stated on page 16, lines 8-14 of the specification as filed, "Figure 7

shows two comparison cycles with each cycle approximately 31 μs in duration. In the first comparison cycle between times 0 μs and 31 μs, the inventive comparator is in the analog configuration between time 0 μs to 5 μs and time 30 μs to 31 μs for a total of 6 μs, and in the digital configuration between time 5 μs and 30 μs for a total of 25 μs. This clearly shows that the comparator is in the power saving digital mode for more than 80% of the comparison cycle time." (emphasis added). Therefore, there is no overlapping as the Office Action suggests, rather, the comparator is in the analog cycle between time 0 μs to 5 μs, in the digital cycle between time 5 μs and 30 μs, and then in the analog cycle between time 30 μs to 31 μs. Thus, there clearly is a cycling function between the analog and digital cycles; i.e., the comparator cycles from analog to digital and back to analog.

Furthermore, as indicated on page 8, lines 19-22 through page 9, lines 1-17 of the specification as originally filed:

> The inventive comparator can be considered analog for part of the cycle and digital for the remainder of the cycle, making it ideal for use in low power applications. The distinction between the analog and digital configurations is determined, in large part, by the presence or absence of static DC current paths as well as the region of operation of the transistors. In the analog configuration, there are static DC current paths present and certain transistors operate in the region known as saturation. In the digital configuration, static DC current paths are absent and the transistors are either operating in the linear (triode) region or cutoff region. When the input signal COMPIN rises from GND toward V_{CC}, the tail current source transistor T1 switches on.
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>
> When the comparator input signal COMPIN is of sufficiently high voltage, the comparator is in the digital

configuration since there is no static DC current flowing and the transistors are operating either in the linear (triode) region or in the cutoff region. Specifically, transistors T1, T2, and T5 are in cutoff while transistors T3 and T4 are in the linear (triode) region. Figures 5 and 6, as will be described later, depict the inventive comparator in the digital configuration.

Moreover, as indicated on page 12, lines 7-18 of the specification as originally filed:

> Figure 3 shows an analog illustration of Figure 2, whereby the transmission gates have been removed and replaced by either an open circuit or short circuit. Inverters INV1 and INV2 have been omitted as well because their outputs are only used as inputs to the now deleted transmission gates. Figure 4 shows an alternate representation of Figure 3, whereby all dangling nets or stubs have been removed to aid in the understanding of the circuit more completely. Figure 4 represents the analog configuration of the inventive comparator of Figure 1, wherein there is static DC current flow, and transistors T2, T3, T4, and T5 operate predominantly in the saturation region. In this configuration, the gate of PMOS tail current transistor T1 is shorted to GND potential which turns it on and allows static DC current to flow from V_{CC} through T1 into the PMOS differential pair transistors T2/T3 and onto GND through current mirror load transistors T4/T5. This analog transformation is essentially a differential pair in an open loop configuration with a current mirror load.

Additionally, as indicated on page 14, lines 1-13 of the specification as originally filed:

> This is further depicted in Figure 5, which shows the digital configuration of Figure 2, and where the transmission gates have been removed and replaced with either an open or short circuit. Moreover, the input signal COMPIN is at an input voltage greater than the external reference voltage V_{REF}. Inverters INV1 and INV2 have been removed for clarity as well. Furthermore, Figure 6 illustrates an alternate representation of Figure 5, whereby all dangling nets or stubs have been removed to aid in the understanding of the circuit more completely. Additionally, in Figure 5, a short circuit exists across transistor T5, which is why it is not present in Figure 6. Also in Figure 5, the V_{REF} pin is unconnected and, therefore, it is not represented in Figure 6. Figure 6 further represents the digital configuration of the inventive comparator of Figure 1 because there are no static DC current paths, and transistors are operating in either the linear (triode) or cutoff regions. As a result, in this configuration,

> minimal power is being dissipated which makes the present invention ideal for low power applications. Furthermore, Figure 6 provides the characteristics of an asymmetric inverting Schmitt trigger.

The above language clearly articulates the analog and digital aspects of the comparator. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw these rejections.

IV. The Prior Art Rejections

Claims 1, 2, 5, 7-11, 14 and 16-18 stand rejected under 35 U.S.C. §102(e) as being anticipated by Thiel (U.S. Patent No. 5,808,496). The Applicant respectfully traverses these rejections based on the following discussion. Thiel teaches an accurate, low-current integrated circuit comparator that includes a differential input stage 10 comprising differential pair transistors 22 and 24, differential pair current mirror transistors 26 and 28, and a constant current source transistor 30. The comparator also includes an hysteresis stage 12 coupled to one of the current mirror transistors; the hysteresis stage comprises an hysteresis mirror transistor 34 and a switching transistor 36. The comparator additionally includes a gain stage 14 comprising a gain transistor 38 and a constant current source transistor 40. Finally, the comparator includes an output stage 15 comprising gain transistor 42 in an open-drain configuration. In the disclosed embodiment, the descending trip threshold is set entirely by the ratios of device geometries, and is therefore very accurate and is independent of temperature, lithography and processing variations. While the ascending trip threshold is related to the ratio of tail current of the differential pair to the transistor gain of the devices in that pair, which quantities are dependent on the device parameters, this relationship is only to the one-half power, and therefore is

relatively small.

As amended, the claimed invention is patentable over Thiel. As suggested in the Office Action, the prior art of record fails to teach a comparator wherein the rise of the input signal switches the tail current source transistor, or a comparator having a plurality of transmission gates wherein the rise of the input signal causes the comparator to appear as a differential pair in an open loop configuration or as an asymmetric inverting Schmitt trigger.

Moreover, there is no mention in Thiel of a cycling function between an analog and digital circuit. The claimed invention includes the ability to control different trip points for the rising and falling edges of an input signal, and provides a comparator which dissipates less power than conventional devices, such as Thiel. Moreover, the claimed invention is ideal for use in low power applications. The ability to raise and lower the trip point of the falling edge of the input signal is important because it allows for adjustment of the amount of hysteresis incorporated into the design. Another important use of an adjustable trip point involves the ability to control the delay between the rising and falling edge transitions at the comparator output signal and, in turn, the pulse width at the output. This use has several applications where the same analog signal is used to generate or derive a digital data signal, as well as a digital clock signal. These features are simply not taught in Thiel.

Moreover, there is nothing in Thiel that teaches or even suggests wherein said comparator cycles between an analog circuit and a digital circuit, and wherein in said analog circuit, one of said at least two transistors is a tail current source transistor, and wherein said input signal rises from ground toward a positive power supply voltage, wherein said rise in said input signal switches said tail current source transistor on, as recited, in part, in amended claims 1 and 10. Therefore, Thiel does not teach the claimed invention. In view of the foregoing, the Examiner is

respectfully requested to reconsider and withdraw these rejections.

V. Formal Matters and Conclusion

Therefore, the Applicant respectfully submits that amended independent claims 1, 10, and 16 are patentable over Thiel. Furthermore, dependent claims 4-9, 11, 13-15, and 17-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define.

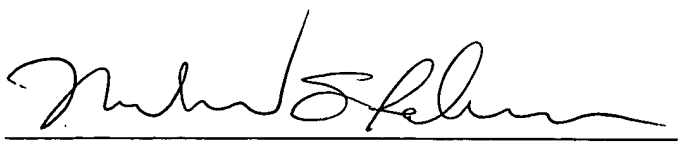
With respect to the objections/rejections to the specifications and claims, the claims have been amended, above, to overcome these objections/rejections. With respect to the objection to the drawings, a Submission of Proposed Drawing Corrections is submitted herewith. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to the specification, claims and drawings.

In view of the foregoing, the Applicant submits that claims 1, 4-11, and 13-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



Dated: October 17, 2003

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